Notice of Allowability	Application No.	Applicant(s)	
	10/815,871	OZAKI, KOJI	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *examiner initiated interview & resulting further amended claims dated 12/27/06 and 1/9/07*.

2. ☒ The allowed claim(s) is/are *1,7-14,20-22*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Surinder Sachar on 12/27/06 and 1/9/07; with the understanding that the caches claimed have line borders which are determined as a function of a pc-relative virtually addressed data and correspondingly considered to comprise lines having a size of greater than two entries as considered supported by the drawings; as all entries within a cache having a line size of two or less words would inherently formulate a logical line boarder of said cache, and thereby would not be considered a patentably distinguishing limitation; whereby:

Claims 1, 14 and 20-22 are further amended; and

Claims 7-13 remain as previously presented; and

Claims 2-6 and 15-19 are canceled.

3. The application has been amended as follows:

Claim 1 (Currently Amended): An information processing apparatus including processor means for executing an operation, the information processing apparatus comprising:

a plurality of functional units for performing functional processes;

storage means for storing said instruction and data for said processor means to execute said operation and including input/output registers for transferring said instruction and data between said processor means and said functional units;

first and second transfer means for transferring said instruction or data between said processor means and said storage means;

first address translation means for translating an instruction virtual address designated by said processor means into a physical address of said storage means; and

second address translation means for translating a data virtual address including the virtual addresses of said data and said input/output registers designated by said processor means into a physical address of said storage means,

wherein each of said first and second transfer means includes an independent respective first and second virtual address space each including virtual addresses, wherein the virtual addresses in the first virtual address space overlap with the virtual addresses in the second virtual address space;

said first and second address translation means translate said virtual address space of said respective first and second transfer means into a single physical address space; [[and]]

the data virtual address space of said input/output registers and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance;

wherein, said first and second transfer means include an instruction bus for transferring said instruction and a data bus for transferring said data; and

a difference between a virtual address of an instruction accompanying an access to said first and second transfer means and a virtual address of data accessed by said instruction is equal to or shorter than a distance which can be directly designated as a relative address by an operand of the instruction; and

further comprising:

a cache, provided for each of said first and second transfer means, said cache using said virtual address as a tag,

wherein said virtual address space includes virtual addresses in such a manner that a border between a virtual address of said instruction and a virtual address of said data becomes a line border of said cache.

Claims 2-6 (Canceled).

Claim 7 (Original): The information processing apparatus according to claim 1,

wherein if a translation unit of an address to be translated by said address translation means contains both a virtual address of said instruction and a virtual address of said data, data included in said translation unit is only constant data.

Claim 8 (Previously Presented): The information processing apparatus according to claim 1,

wherein said address translation means translates said virtual address space of said respective first and second transfer means into said single physical address space having mutually non-overlapping addresses.

Claim 9 (Original): The information processing apparatus according to claim 1,

wherein said storage means includes a write inhibited area and a write permitted area; and

virtual addresses of both said write inhibited area and said write permitted area are disposed in a virtual address space in a range that can be directly designated as a relative address by an operand of an instruction accompanying an access to said storage means.

Claim 10 (Original): The information processing apparatus according to claim 1,

wherein said storage means includes at least one input/output (I/O) register; and

a difference between a virtual address of said instruction accompanying an access to said I/O register and a virtual address representative of said I/O register is equal to or shorter than a distance that can be directly designated as a relative address by an operand of said instruction.

Claim 11 (Original): The information processing apparatus according to claim 10,

wherein a virtual address representative of a same I/O register is divided and disposed in a plurality of areas of said virtual address space.

Claim 12 (Original): The information processing apparatus according to claim 1,

wherein said address translation means translates upper n bits of said virtual address of (n + m) bits, and at least one bit or more of the translated upper n bits is exchanged with at least one or more bits of the remaining m bits, thereby translating said virtual address into said physical address.

Claim 13 (Original): The information processing apparatus according to claim 1,

wherein said address translation means translates upper n bits of said virtual address of (n + m) bits, and at least one bit or more of the remaining lower m bits is exchanged with another one bit or more of the remaining lower m bits, thereby translating said virtual address into said physical address.

Claim 14 (Currently Amended): An information processing method for an information processing apparatus, the information processing apparatus including:

processor means for executing an operation;

a plurality of functional units for performing functional processes;

storage means for storing said instruction and data for said processor means to execute said operation and including input/output registers for transferring said instruction and data between said processor means and said functional units;

first and second transfer means for transferring said instruction or data between said processor means and said storage means;

first address translation means for translating an instruction virtual address designated by said processor means into a physical address of said storage means; and

second address translation means for translating a data virtual address including the virtual addresses of said data and said input/output registers designated by said processor means into a physical address of said storage means,

wherein each of said first and second transfer means includes an independent respective first and second virtual address space each including virtual addresses, wherein the virtual addresses in the first virtual address space overlap with the virtual addresses in the second virtual address space;

first and second address translation means include a translation step of translating said virtual address space of said respective first and second transfer means into a single physical address space; [[and]]

the data virtual address space of said input/output registers and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance;

wherein, said first and second transfer means include an instruction bus for transferring said instruction and a data bus for transferring said data; and

determining a difference between a virtual address of an instruction accompanying an access to said first and second transfer means and a virtual address of data accessed by said instruction that is equal to or shorter than a distance which can be directly designated as a relative address by an operand of the instruction; and

further comprising:

a cache, provided for each of said first and second transfer means, said cache using said virtual address as a tag,

wherein determining a cache line border of as a function of said difference between virtual addresses such that the border between a virtual address of said instruction and a virtual address of said data becomes the line border of said cache.

Claim 15-19 (Canceled).

Claim 20 (Currently Amended): An imaging apparatus comprising:

imaging means for taking an image of an object;

encoding means for encoding image data of the object taken with said imaging means;

processor means for executing an operation of designating an instruction or data for said encoding means to encode said image data; and

wherein the imaging apparatus further comprises:

a plurality of functional units for performing functional processes;

storage means for storing said instruction and data for said processor means to execute said operation and including input/output registers for transferring said instruction and data between said processor means and said functional units;

first and second transfer means for transferring said instruction or data between said processor means and said storage means;

first address translation means for translating an instruction virtual address designated by said processor means into a physical address of said storage means; and

second address translation means for translating a data virtual address including the virtual addresses of said data and said input/output registers designated by said processor means into a physical address of said storage means,

wherein each of said first and second transfer means includes an independent respective first and second virtual address space each including virtual addresses, wherein virtual addresses in the first virtual address space overlap with the virtual addresses in the second virtual address space;

said first and second address translation means translate said virtual address space of said respective first and second transfer means into a single physical address space;

the data virtual address space of said input/output registers and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance[[, and]];

said encoding means encodes said image data in accordance with said instruction or data in said storage means corresponding to an address designated by said processor means and translated by said address translation means;

wherein, said first and second transfer means include an instruction bus for transferring said instruction and a data bus for transferring said data; and

a difference between a virtual address of an instruction accompanying an access to said first and second transfer means and a virtual address of data accessed by said

instruction is equal to or shorter than a distance which can be directly designated as a relative address by an operand of the instruction; and

further comprising:

a cache, provided for each of said first and second transfer means, said cache using said virtual address as a tag,

wherein said virtual address space includes virtual addresses in such a manner that a border between a virtual address of said instruction and a virtual address of said data becomes a line border of said cache.

Claim 21 (Currently Amended): An information processing apparatus including a processor for executing an operation, the information processing apparatus comprising:

a plurality of functional units for performing functional processes;

a storage for storing said instruction and data for said processor to execute said operation and including input/output registers for transferring said instruction and data between said processor and said functional units;

first and second transfer sections for transferring said instruction or data between said processor and said storage;

a first address translator for translating a virtual address designated by said processor into a physical address of said storage; and

a second address translator for translating a data virtual address including the virtual addresses of said data and said input/output registers designated by said processor into a physical address of said storage means,

wherein each of said first and second transfer sections includes an independent respective first and second virtual address space each including virtual addresses, wherein virtual addresses in the first virtual address space overlap with the virtual addresses in the second virtual address space;

said first and second address translators translate said virtual address space of said respective first and second transfer sections into a single physical address space; [[and]]

the data virtual address space of said input/output registers and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance;

wherein, said first and second transfer means include an instruction bus for transferring said instruction and a data bus for transferring said data; and

a difference between a virtual address of an instruction accompanying an access to said first and second transfer means and a virtual address of data accessed by said instruction is equal to or shorter than a distance which can be directly designated as a relative address by an operand of the instruction; and

further comprising:

a cache, provided for each of said first and second transfer means, said cache using said virtual address as a tag,

wherein said virtual address space includes virtual addresses in such a manner that a border between a virtual address of said instruction and a virtual address of said data becomes a line border of said cache.

Claim 22 (Currently Amended): An imaging apparatus comprising:

an imaging section for taking an image of an object;

an encoder for encoding image data of the object taken with said imaging section;

a processor for executing an operation of designating an instruction or data for said encoder to encode said image data;

wherein the imaging apparatus further comprises:

a plurality of functional units for performing functional processes;

a storage means storing said instruction and data for said processor to execute said operation and including input/output registers for transferring said instruction and data between said processor and said functional units;

first and second transfer sections for transferring said instruction or data between said processor and said storage;

a first address translator for translating a virtual address designated by said processor into a physical address of said storage; and

a second address translator for translating a data virtual address including the virtual addresses of said data and said input/output registers designated by said processor into a physical address of said storage means,

wherein each of said first and second transfer sections includes an independent respective first and second virtual address space each including virtual addresses, wherein the virtual addresses in the first virtual address space overlap with the virtual addresses in the second virtual address space;

said first and second address translators translate said virtual address space of said respective first and second transfer sections into a single physical address space; [[and]]

the data virtual address space of said input/output registers and data are divided and disposed in a plurality of address areas so that the virtual addresses of an instruction and corresponding data and input/output registers are disposed at a near distance[[.]];

said encoder encodes said image data in accordance with said instruction or data in said storage corresponding to an address designated by said processor and translated by said address translation section;

wherein, said first and second transfer means include an instruction bus for transferring said instruction and a data bus for transferring said data; and

a difference between a virtual address of an instruction accompanying an access to said first and second transfer means and a virtual address of data accessed by said instruction is equal to or shorter than a distance which can be directly designated as a relative address by an operand of the instruction; and

further comprising:

a cache, provided for each of said first and second transfer means, said cache using said virtual address as a tag,

wherein said virtual address space includes virtual addresses in such a manner that a border between a virtual address of said instruction and a virtual address of said data becomes a line border of said cache.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PIERRE BATAILLE
PRIMARY EXAMINER
11/17/07